650V SuperJunction Power MOSFET

Features

- Extremely Low Gate Charge
- Excellent Output Capacitance (C_{oss}) Profile
- Fast Switching Capability
- 100% UIS Tested, 100% Rg Tested
- Pb-free Lead Plating
- Halogen-free and RoHS-compliant

Product Summary

Parameter	Value	Unit
V_{DS}	650	V
$V_{GS(th)\_Typ}$	3.5	V
I_D (@ V_{GS} = 10V) (1)	10.4	A
$R_{DS(ON)\_Typ}$ (@ V_{GS} = 10V)	370	mΩ
E_{oss}@400V	2.2	μJ

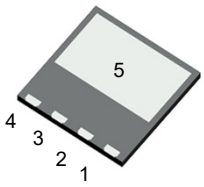
Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar
- Lighting / Charger / Adapter

DFN8080-4L

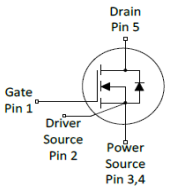
Top View

Bottom View



Pin Configuration

Top View

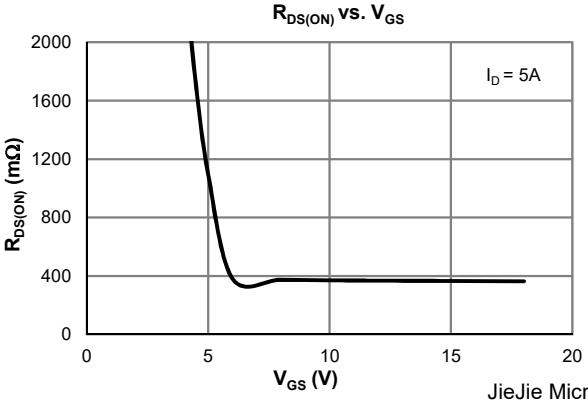


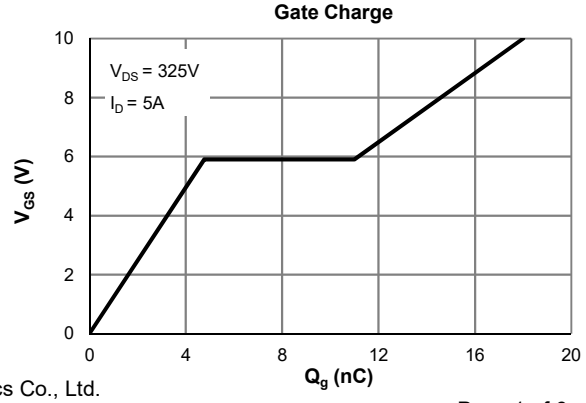
Ordering Information

Device	Package	# of Pins	Marking	MSL	T_J (°C)	Media	Quantity (pcs)
JMH65R430APLN-13	DFN8080-4L	4	H65R430A	1	-55 to 150	13-inch Reel	3000

Absolute Maximum Ratings (@ T_A = 25°C unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DS}	650	V
Gate-to-Source Voltage		V_{GS}	±30	V
Continuous Drain Current (1)	T_C = 25°C	I_D	10.4	A
	T_C = 100°C		6.6	
Pulsed Drain Current (2)		I_{DM}	42	A
Avalanche Current (3)		I_{AS}	6.0	A
Avalanche Energy (3)		E_{AS}	180	mJ
Power Dissipation (4)	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C





Electrical Characteristics (@ T_J = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
STATIC PARAMETERS						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 250μA, V_{GS} = 0V	650			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650V, V_{GS} = 0V			1.0	μA
Gate-Body Leakage Current	I_{GSS}	V_{DS} = 0V, V_{GS} = ±30V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2.5	3.5	4.5	V
Static Drain-Source ON-Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 5A		370	430	mΩ
Diode Forward Voltage	V_{SD}	I_S = 1A, V_{GS} = 0V		0.75	1.0	V
Diode Continuous Current	I_S	T_C = 25°C			125	A
DYNAMIC PARAMETERS (5)						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 100V, f = 1MHz		703		pF
Output Capacitance	C_{oss}			25		pF
Reverse Transfer Capacitance	C_{rss}			2.1		pF
Effective output capacitance, energy relate	$C_{o(er)}$	V_{GS} = 0V, V_{DS} = 0 to 400V		28		pF
Effective output capacitance, time related	$C_{o(tr)}$			119		pF
Gate Resistance	R_g	V_{GS} = 0V, V_{DS}= 0V, f = 1MHz		8.5		Ω
SWITCHING PARAMETERS (5)						
Total Gate Charge (@ V_{GS} = 10V)	Q_g	V_{GS} = 0 to 10V V_{DS} = 325V, I_D = 5A		18.4		nC
Total Gate Charge (@ V_{GS} = 6.0V)	Q_g			11.0		nC
Gate Source Charge	Q_{gs}			4.8		nC
Gate Drain Charge	Q_{gd}			7.6		nC
Turn-On DelayTime	$t_{D(on)}$	V_{GS} = 10V, V_{DS} = 325V R_L = 65Ω, R_{GEN} = 6Ω		27		ns
Turn-On Rise Time	t_r			16.8		ns
Turn-Off DelayTime	$t_{D(off)}$			104		ns
Turn-Off Fall Time	t_f			31		ns
Body Diode Reverse Recovery Time	t_{rr}	I_F = 5A, dI_F/dt = 100A/μs		239		ns
Body Diode Reverse Recovery Charge	Q_{rr}	I_F = 5A, dI_F/dt = 100A/μs		2513		nC
Peak Diode Recovery Voltage Slope	dv/dt	$I_F \leqslant$ 10A, di/dt = 200A/us, V_{DS} = 400V		15		V/ns
MOSFET dv/dt Ruggedness	dv/dt	V_{DS} = 0...400V		50		V/ns

Thermal Performance

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	45	54	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.0	1.2	°C/W

Notes:

1. Computed continuous current assumes the condition of T_{J_Max} while the actual continuous current depends on the thermal & electro-mechanical application board design.
2. This single-pulse measurement was taken under T_{J_Max} = 150°C.
3. This single-pulse measurement was taken under the following condition [L = 10mH, V_{GS} = 10V, V_{DS} = 50V] while its value is limited by T_{J_Max} = 150°C.
4. The power dissipation P_D is based on T_{J_Max} = 150°C.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Electrical & Thermal Characteristics

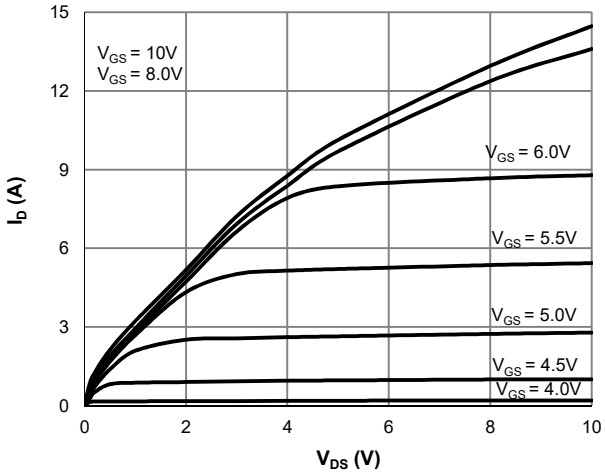


Figure 1: Saturation Characteristics

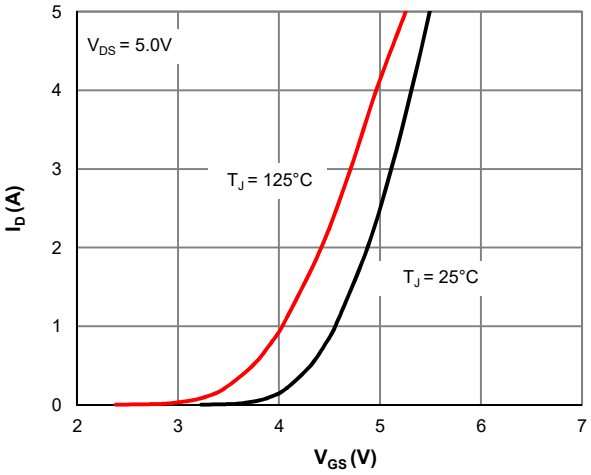


Figure 2: Transfer Characteristics

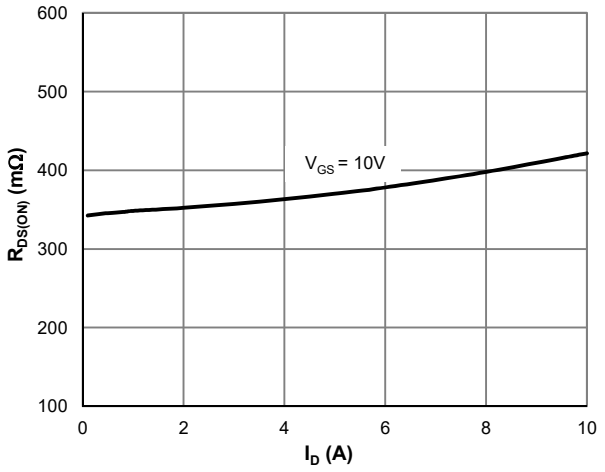


Figure 3: $R_{DS(ON)}$ vs. Drain Current

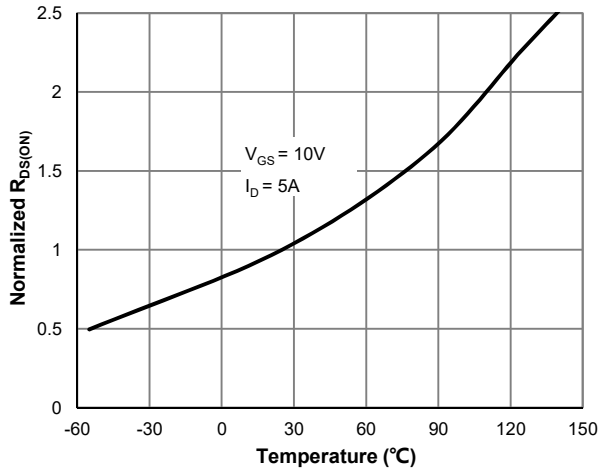


Figure 4: $R_{DS(ON)}$ vs. Junction Temperature

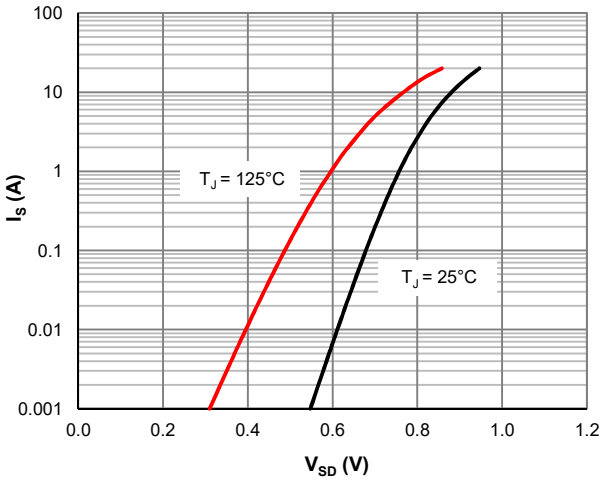


Figure 7: Body-Diode Characteristics

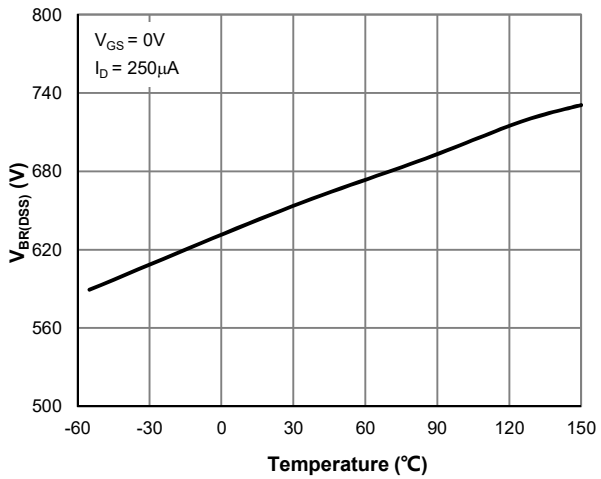


Figure 6: $V_{BR(DSS)}$ vs. Junction Temperature

Typical Electrical & Thermal Characteristics

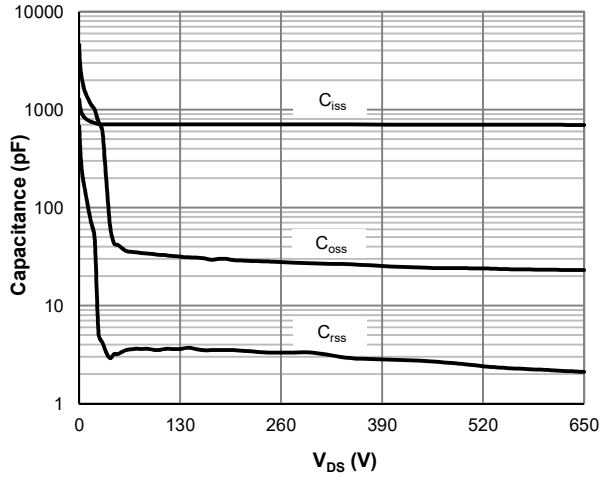


Figure 8: Capacitance Characteristics

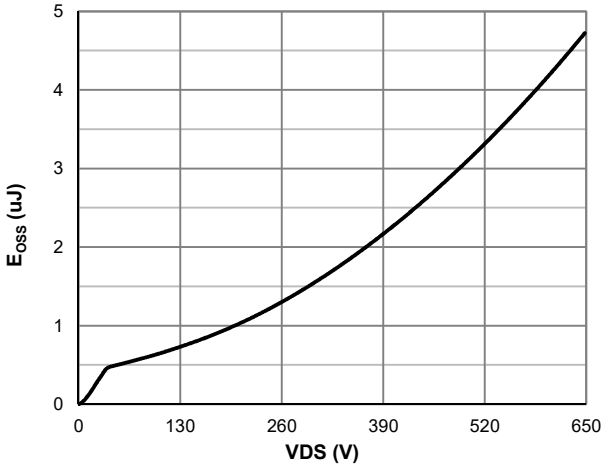


Figure 8: Coss Stoted Energy

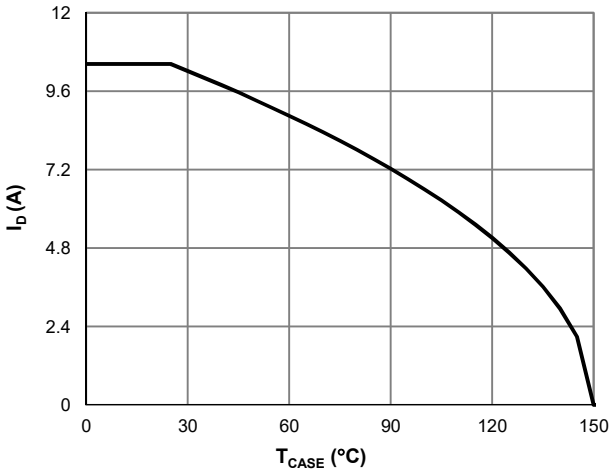


Figure 9: Current De-rating

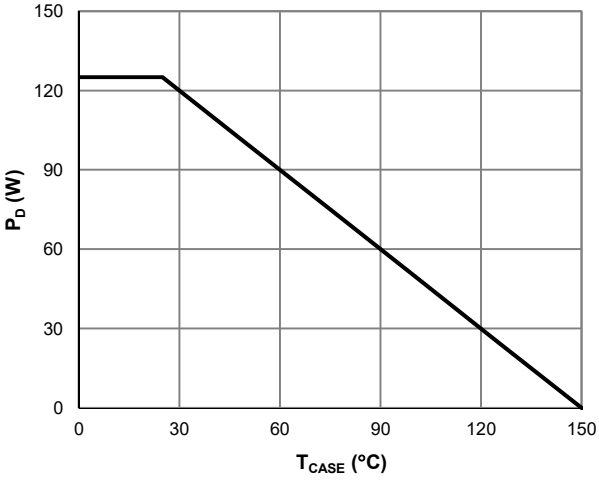


Figure 10: Power De-rating

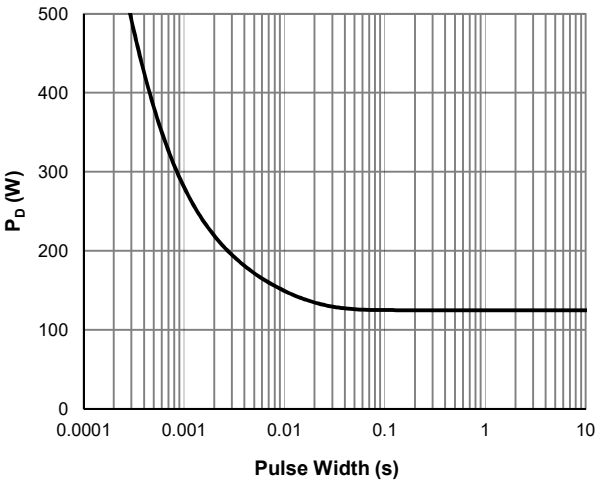


Figure 11: Single Pulse Power Rating, Junction-to-Case

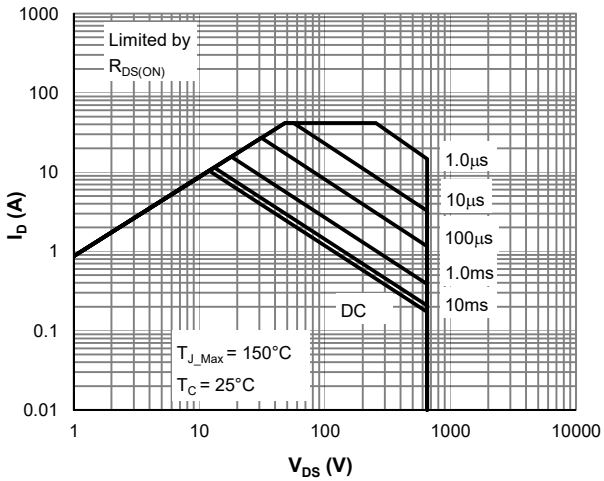


Figure 12: Maximum Safe Operating Area

Typical Electrical & Thermal Characteristics

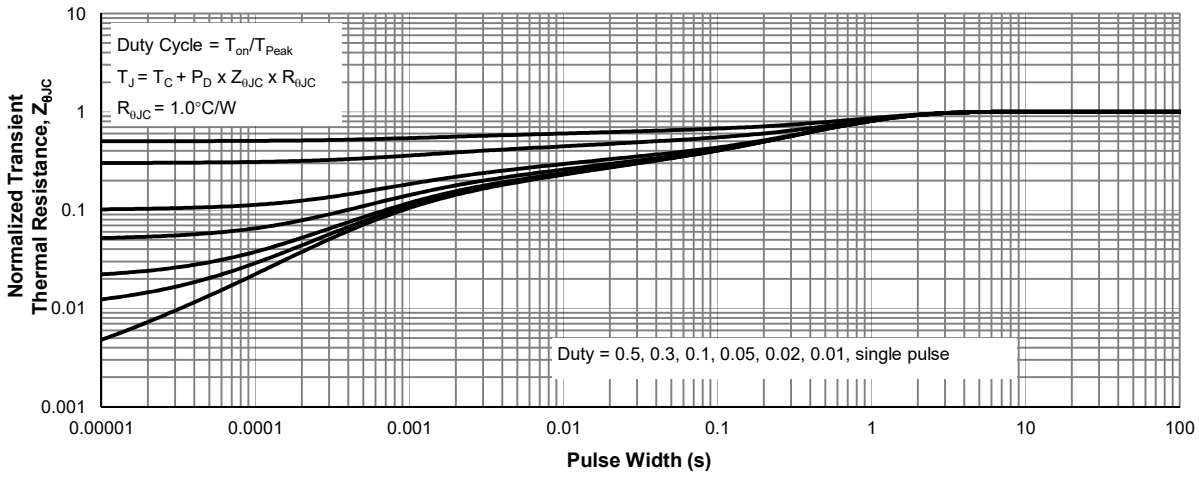
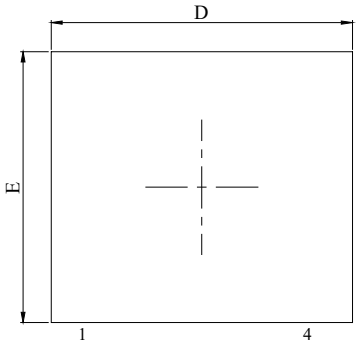


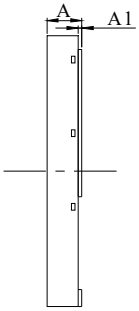
Figure 13: Normalized Maximum Transient Thermal Impedance

DFN8080-4L Package Information

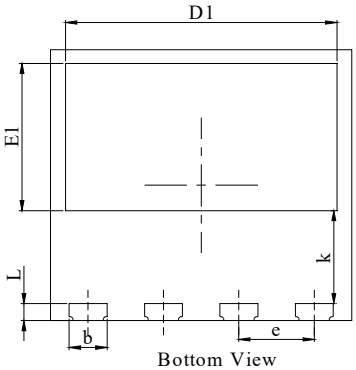
Package Outlines



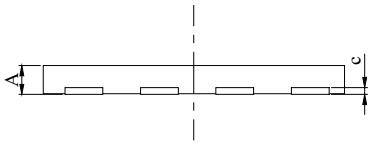
Top View



Side View



Bottom View



Front View

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	--	--	0.05
b	0.95	1.00	1.05
c	--	0.20	--
D	7.90	8.00	8.10
D1	7.10	7.20	7.30
E	7.90	8.00	8.10
E1	4.25	4.35	4.45
L	0.40	0.50	0.60
k	2.75		
e	2.00 BSC		

Recommended Soldering Footprint