

Description

JMT P-channel Enhancement Mode Power MosFET

Features

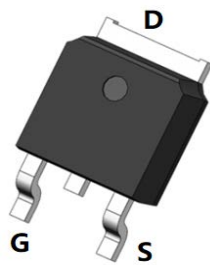
- -30V, -50A
- $R_{DS(ON)} < 9.2m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} < 13.4m\Omega @ V_{GS} = -4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

- Load Switch
- PWM Application
- Power Management



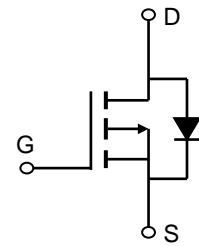
100% UIS TESTED!
100% ΔVds TESTED!



TO-252-3L(DPAK) Top View



Marking and Pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
JMTK50P03A	JMTK50P03A	TAPING	TO-252-3L	13"	2500	25000

Absolute Maximum Ratings (@ $T_C = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	-30	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	-50
		$T_C = 100^\circ C$	-22
I_{DM}	Pulsed Drain Current ⁽¹⁾	-200	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	100	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	52
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	29	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.4	
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	°C



Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = -250μA, V _{GS} = 0V	-30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -30V, V _{GS} = 0V	-	-	-1.0	μA
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-1.0	-1.7	-2.5	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽⁴⁾	V _{GS} = -10V, I _D = -12A	-	7.1	9.2	mΩ
		V _{GS} = -4.5V, I _D = -8A	-	10.3	13.4	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz	-	2252	-	pF
C _{oss}	Output Capacitance		-	306	-	pF
C _{rss}	Reverse Transfer Capacitance		-	222	-	pF
Q _g	Total Gate Charge	V _{GS} = 0 to -10V V _{DS} = -15V, I _D = -10A	-	41	-	nC
Q _{gs}	Gate Source Charge		-	7	-	nC
Q _{gd}	Gate Drain("Miller") Charge		-	10	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On DelayTime	V _{GS} = -10V, V _{DD} = -15V I _D = -10A, R _{GEN} = 3Ω	-	6	-	ns
t _r	Turn-On Rise Time		-	2	-	ns
t _{d(off)}	Turn-Off DelayTime		-	90	-	ns
t _f	Turn-Off Fall Time		-	52	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-50	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-200	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S = -30A	-	-	-1.2	V
t _{rr}	Body Diode Reverse Recovery Time	I _F = -10A, di/dt = 100A/us	-	15	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	6	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2. EAS condition: Starting T_J=25C, V_{DD}=-15V, V_G=-10V, R_G=25ohm, L=0.5mH, I_{AS}=-20A
3. R_{θJA} is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB
4. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 0.5%.

Typical Performance Characteristics

Figure 1: Output Characteristics

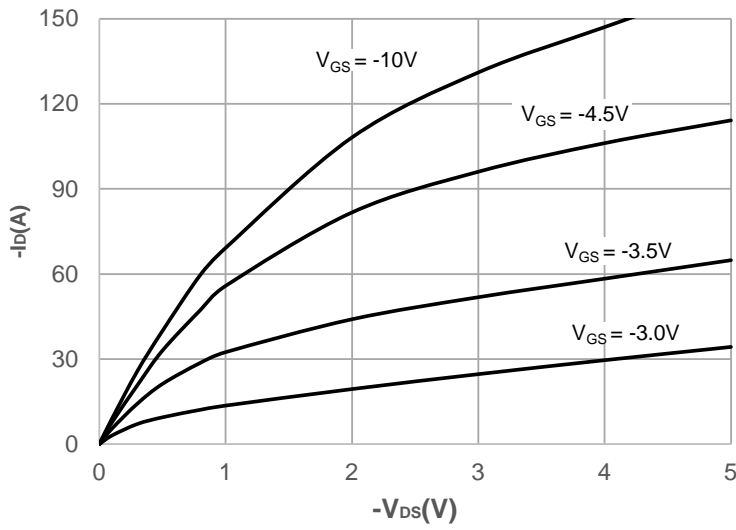


Figure 2: Typical Transfer Characteristics

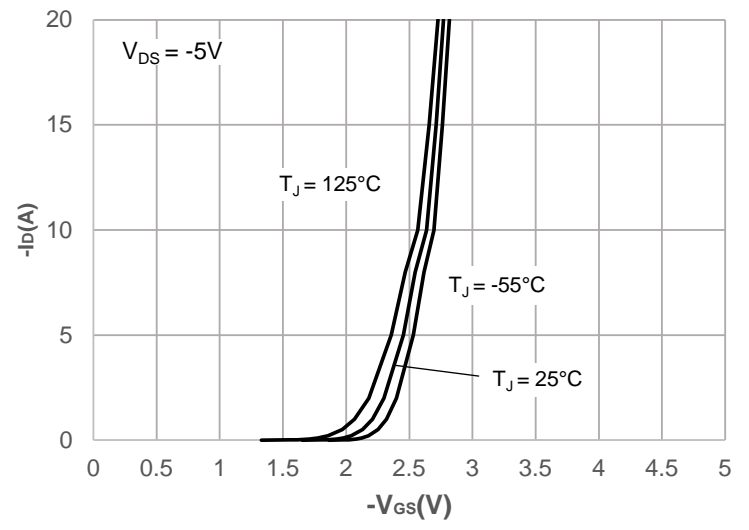


Figure 3: On-resistance vs. Drain Current

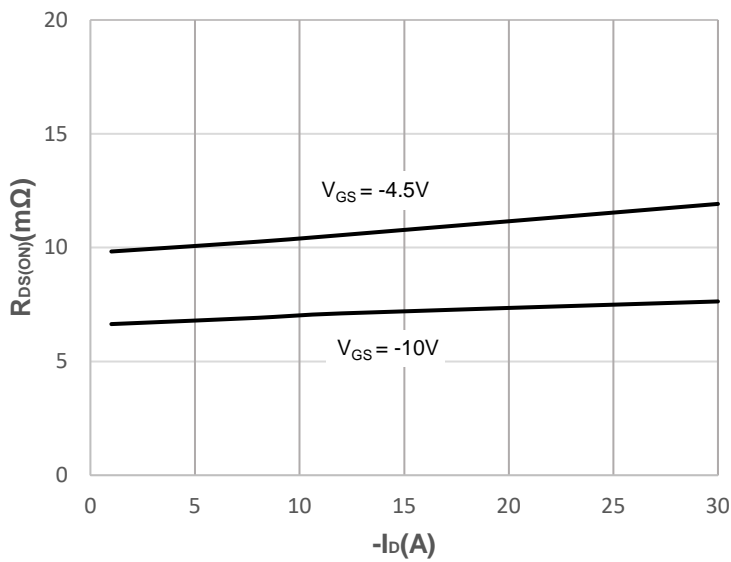


Figure 4: Body Diode Characteristics

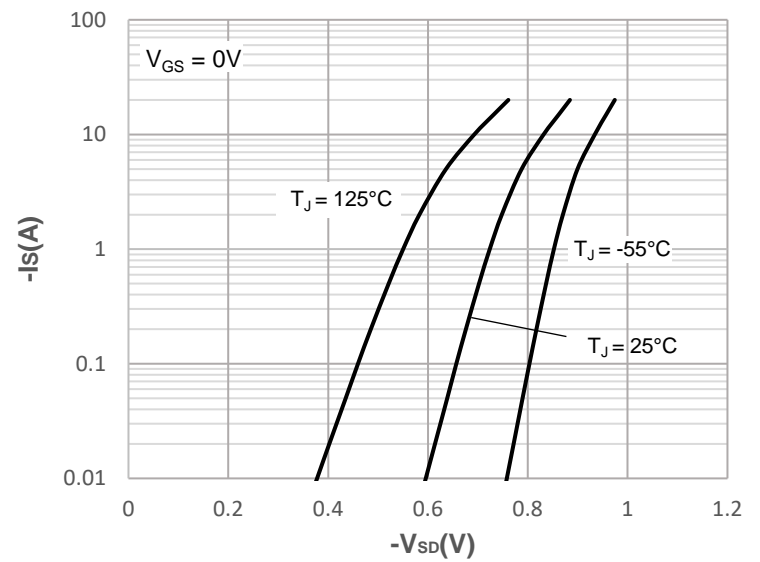


Figure 5: Gate Charge Characteristics

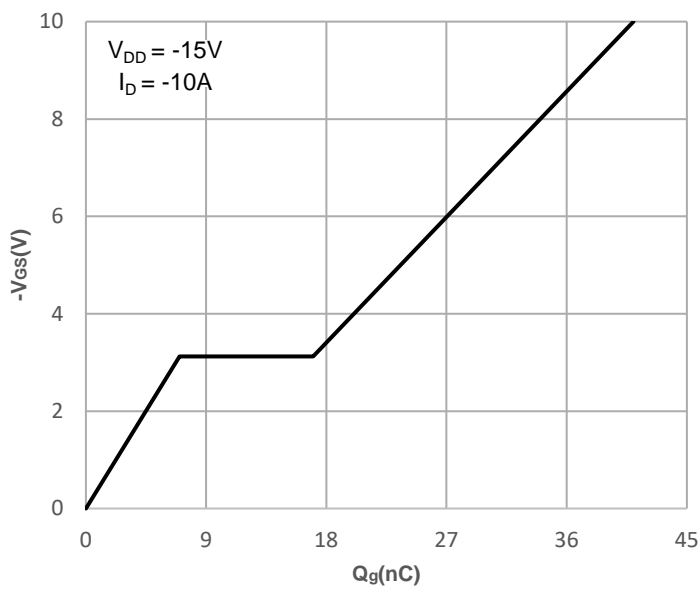
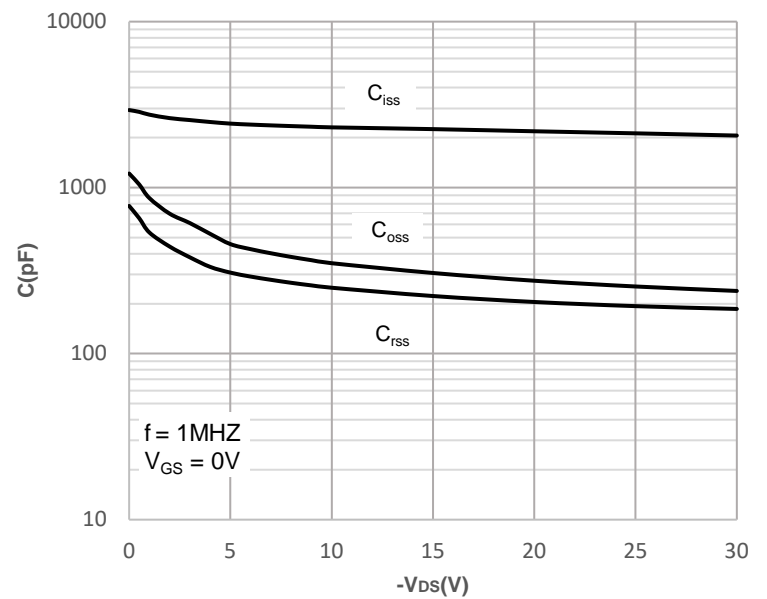


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

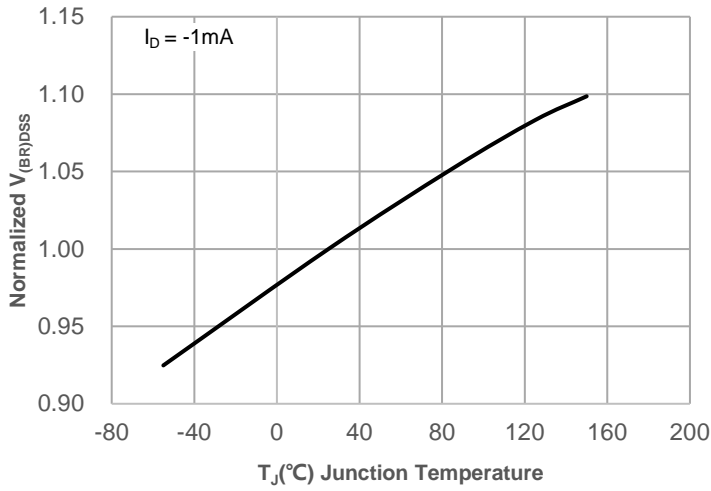


Figure 8: Normalized on Resistance vs. Junction Temperature

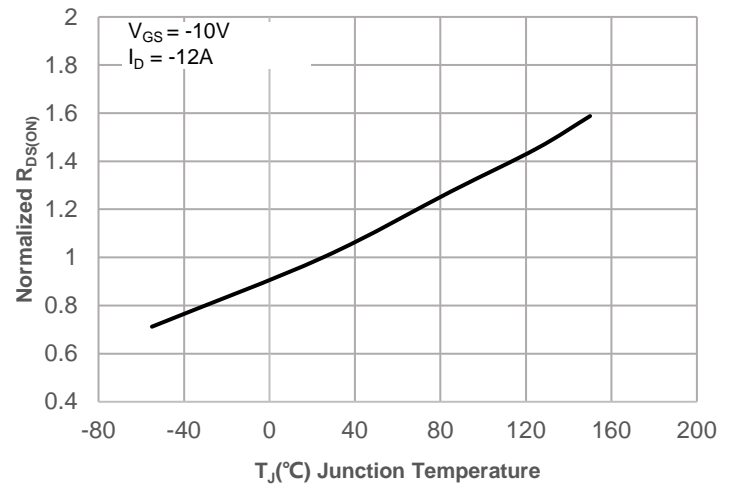


Figure 9: Maximum Safe Operating Area

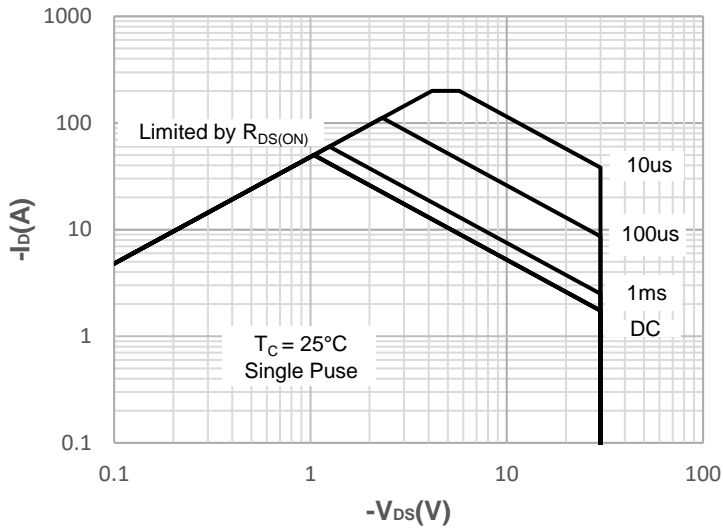


Figure 10: Maximum Continuous Driant Current vs. Case Temperature

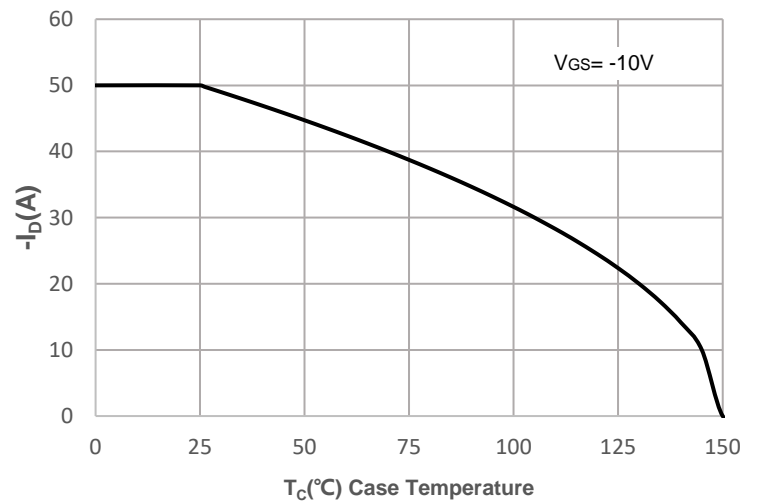


Figure 11: Normalized Maximum Transient Thermal Impedance

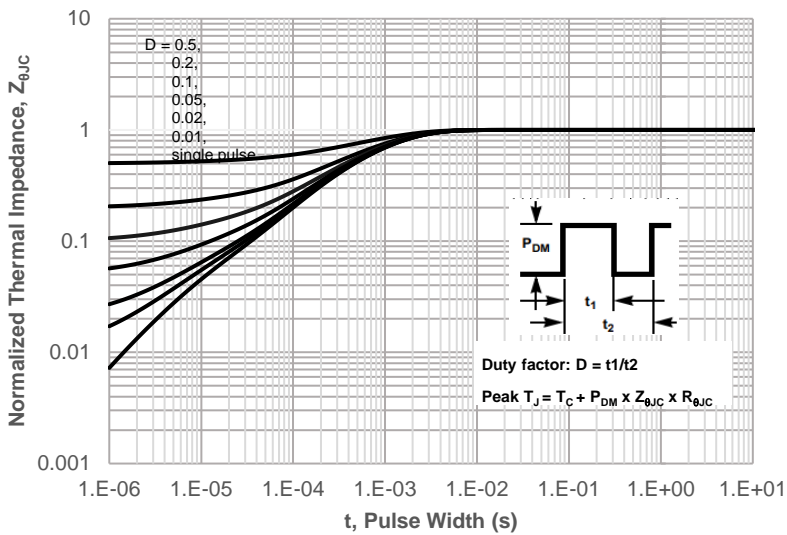
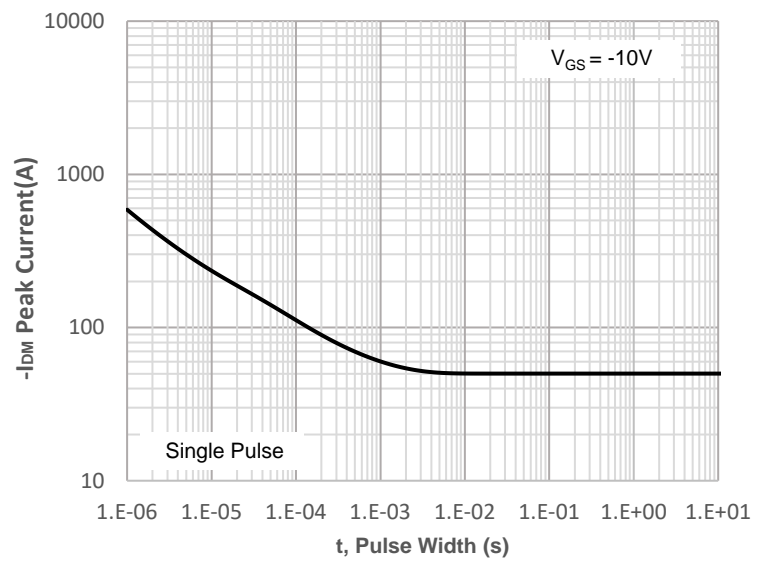


Figure 12: Peak Current Capacity



Test Circuit

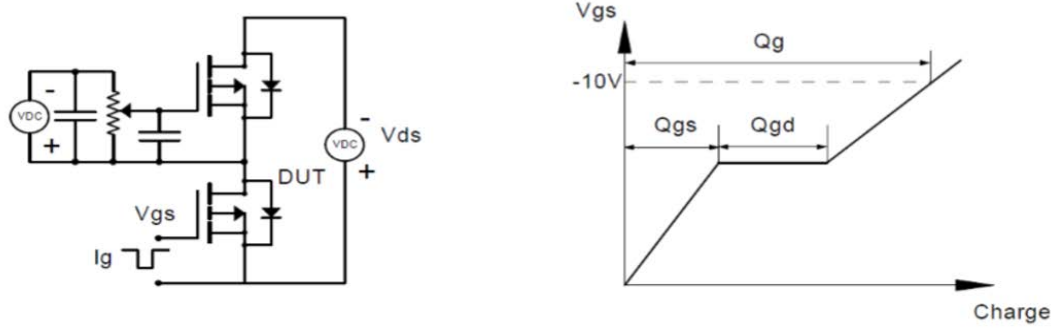


Figure 1: Gate Charge Test Circuit & Waveform

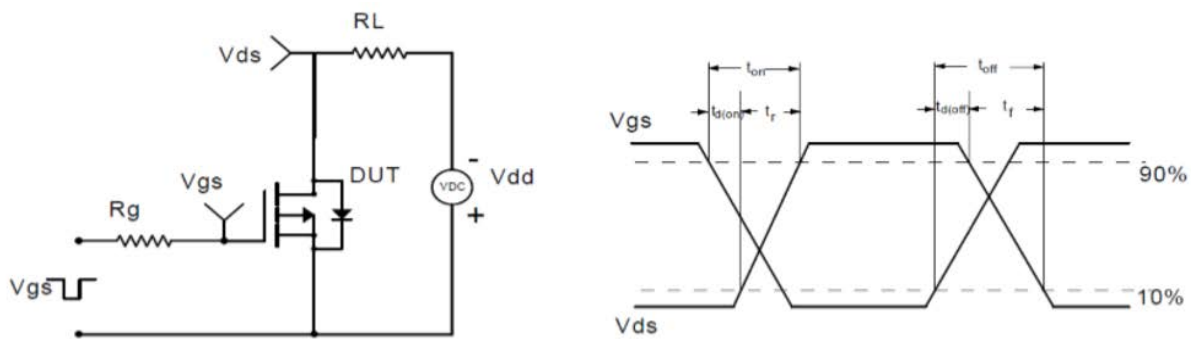


Figure 2: Resistive Switching Test Circuit & Waveform

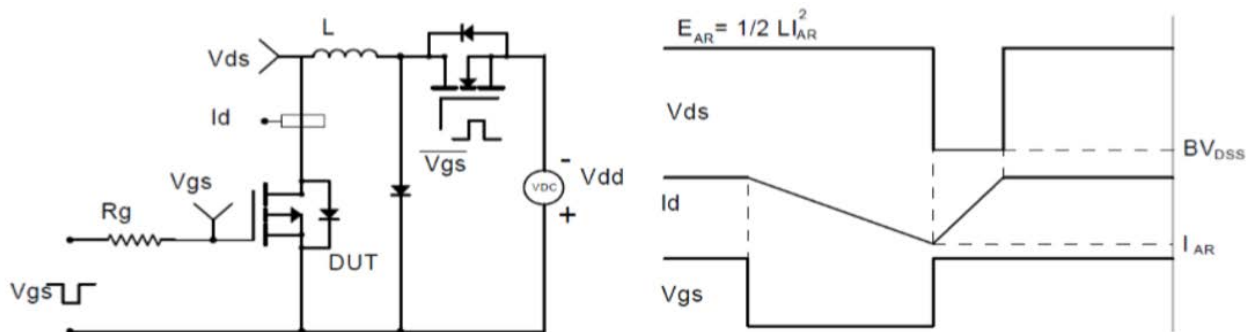


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

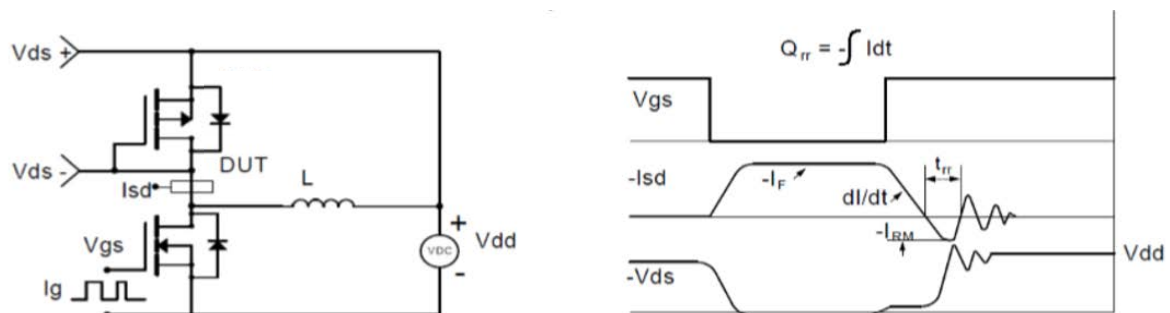
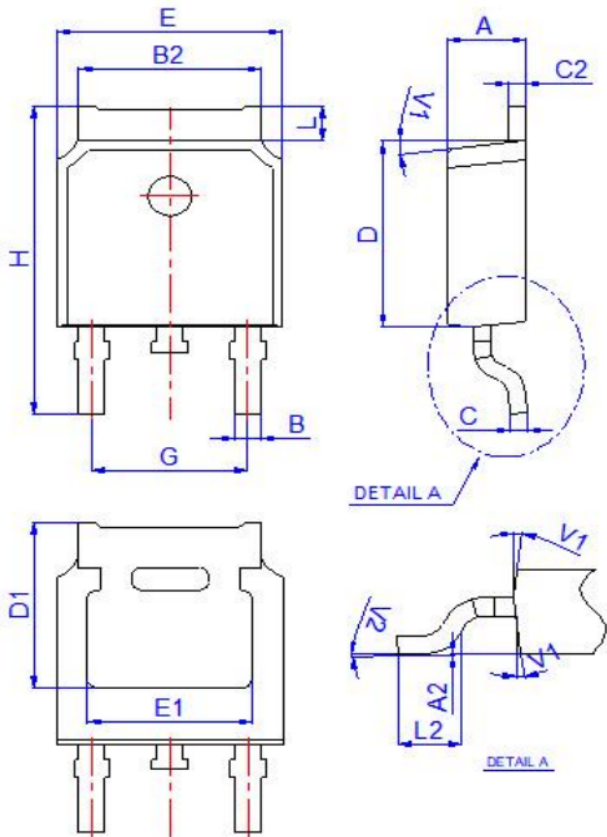


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(TO-252-3L)



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

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