

Description

JMT Dual N-channel Enhancement Mode Power MOSFET

Features

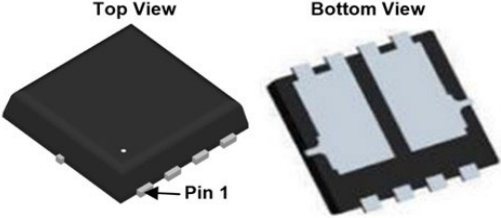
- 40V, 20A
 $R_{DS(ON)} < 19.2m\Omega @ V_{GS} = 10V$
 $R_{DS(ON)} < 25.4m\Omega @ V_{GS} = 4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

- Load Switch
- PWM Application
- Power Management

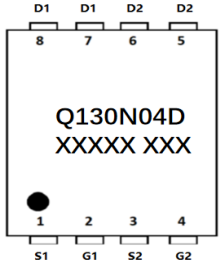


100% UIS TESTED!
100% ΔVds TESTED!



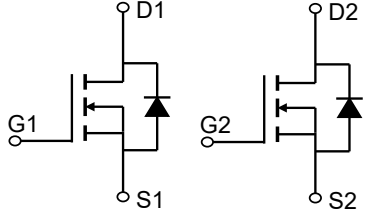
Top View Bottom View

PDFN3x3-8L-D



Q130N04D
XXXXX XXX

Marking and Pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
Q130N04D	JMTQ130N04D	TAPING	PDFN3x3-8L-D	13"	5000	50000

Absolute Maximum Ratings (@ $T_C = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	40	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	20
		$T_C = 100^\circ C$	13
I_{DM}	Pulsed Drain Current ⁽¹⁾	80	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	30	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	50
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	61	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.5	
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ C$



Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = 250μA, V _{GS} = 0V	40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 40V, V _{GS} = 0V	-	-	1.0	μA
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1.3	2	2.3	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽⁴⁾	V _{GS} = 10V, I _D = 20A	-	14.8	19.2	mΩ
		V _{GS} = 4.5V, I _D = 10A	-	19.5	25.4	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 20V, f = 1MHz	-	1342	-	pF
C _{oss}	Output Capacitance		-	87	-	pF
C _{rss}	Reverse Transfer Capacitance		-	72	-	pF
Q _g	Total Gate Charge	V _{GS} = 0 to 10V V _{DS} = 20V, I _D = 10A	-	26	-	nC
Q _{gs}	Gate Source Charge		-	6	-	nC
Q _{gd}	Gate Drain("Miller") Charge		-	5	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On DelayTime	V _{GS} = 10V, V _{DD} = 20V I _D = 10A, R _{GEN} = 3Ω	-	7	-	ns
t _r	Turn-On Rise Time		-	11	-	ns
t _{d(off)}	Turn-Off DelayTime		-	26	-	ns
t _f	Turn-Off Fall Time		-	5	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	20	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	80	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S = 20A	-	-	1.2	V
t _{rr}	Body Diode Reverse Recovery Time	I _F = 10A, di/dt = 100A/us	-	10	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	6	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting T_J=25°C, V_{DD}=20V, V_G=10V, R_G=25ohm, L=0.5mH, I_{AS}=11A
 3. R_{θJA} is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB
 4. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 0.5%.

Typical Performance Characteristics

Figure 1: Output Characteristics

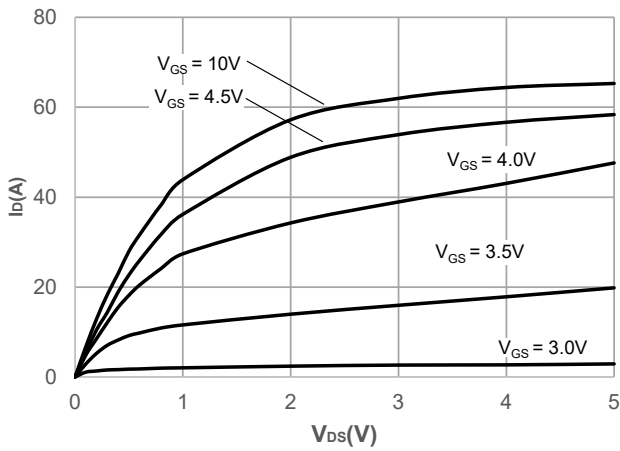


Figure 2: Typical Transfer Characteristics

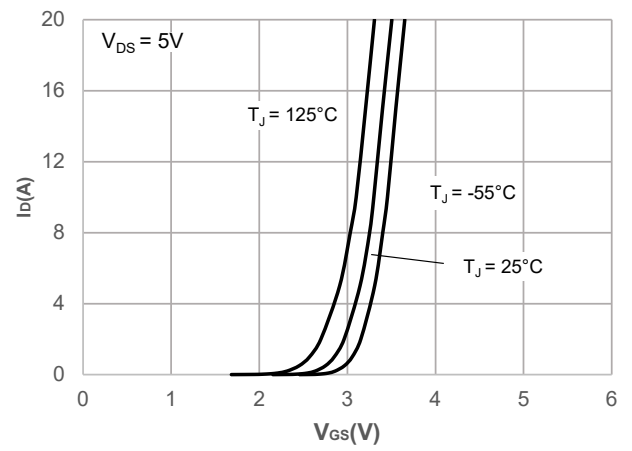


Figure 3: On-resistance vs. Drain Current

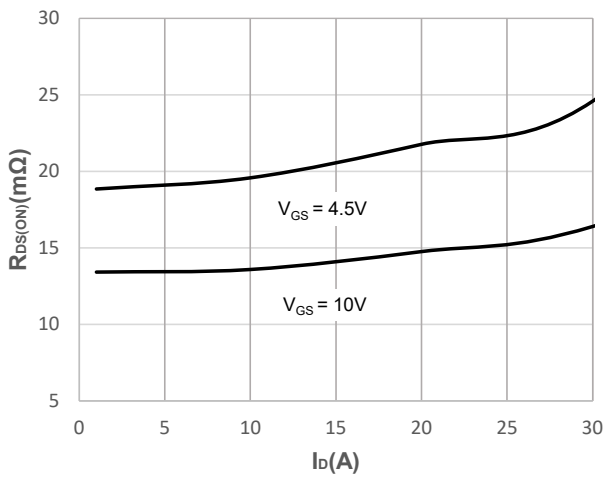


Figure 4: Body Diode Characteristics

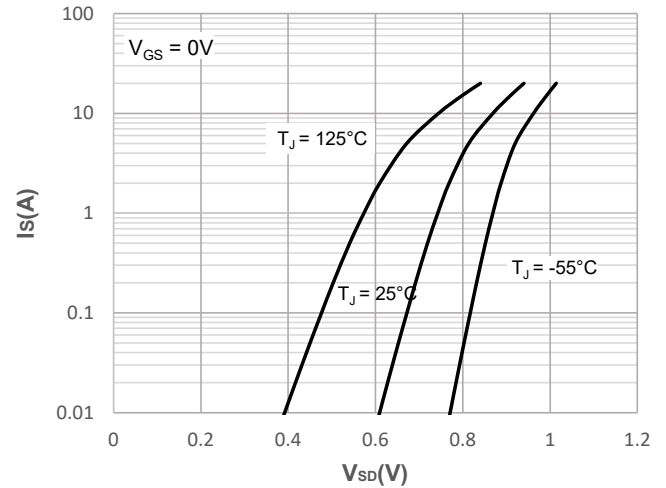


Figure 5: Gate Charge Characteristics

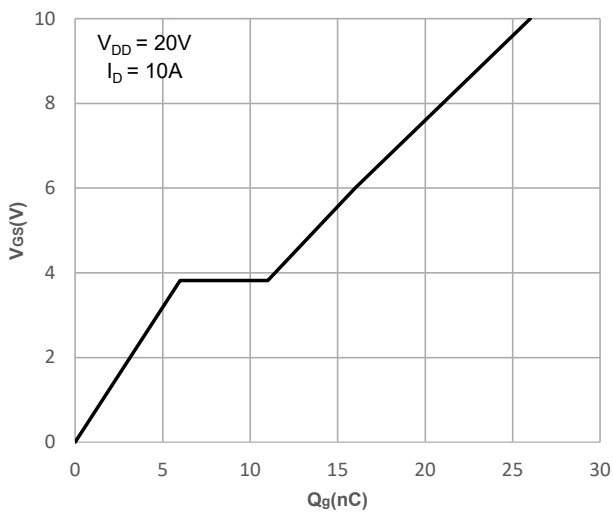
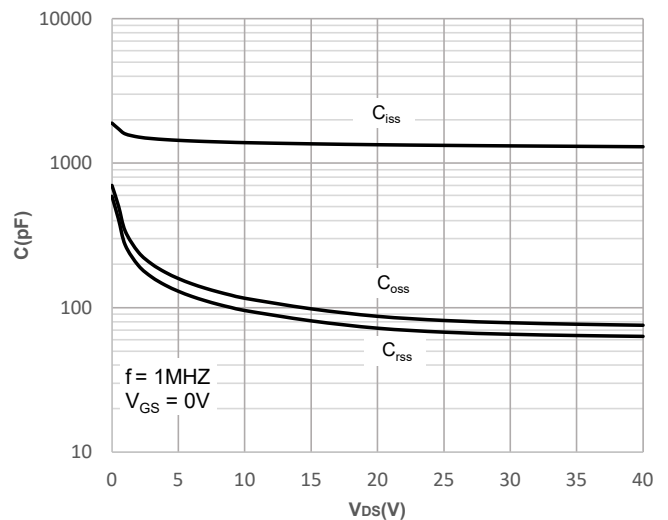


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

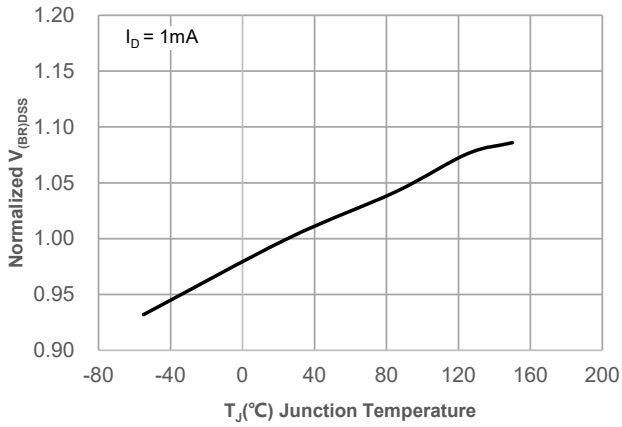


Figure 8: Normalized on Resistance vs. Junction Temperature

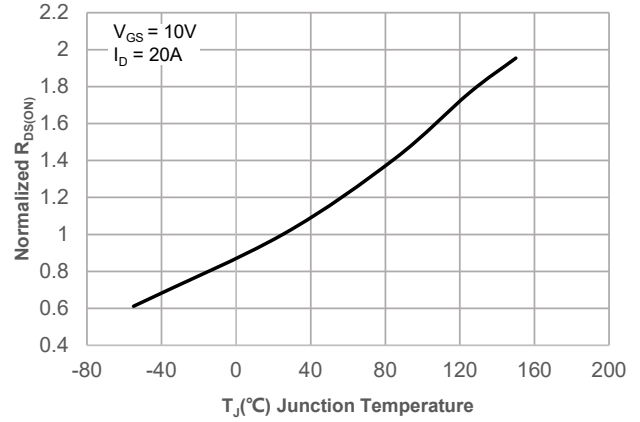


Figure 9: Maximum Safe Operating Area

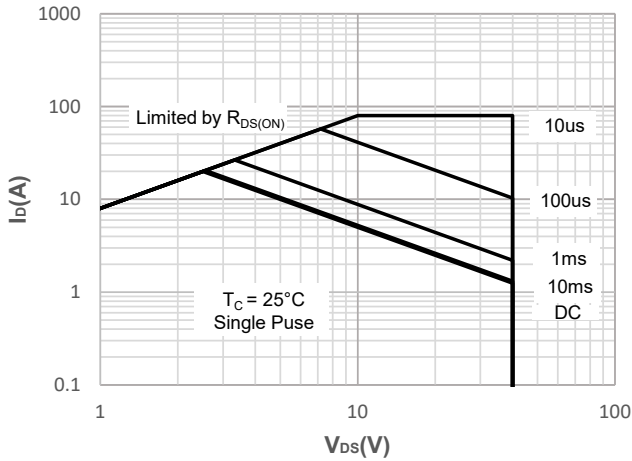


Figure 10: Maximum Continuous Driand Current vs. Case Temperature

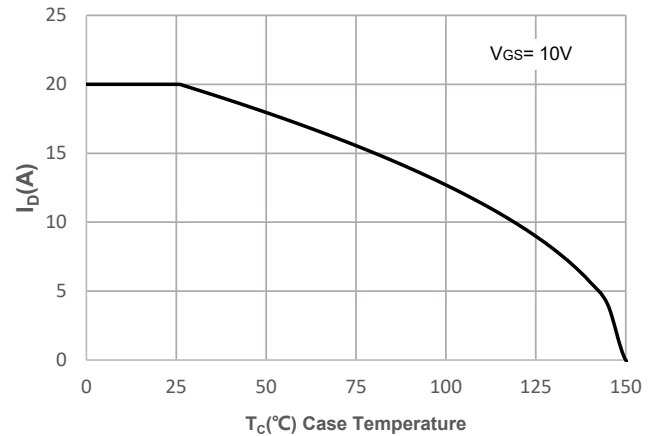


Figure 11: Normalized Maximum Transient Thermal Impedance

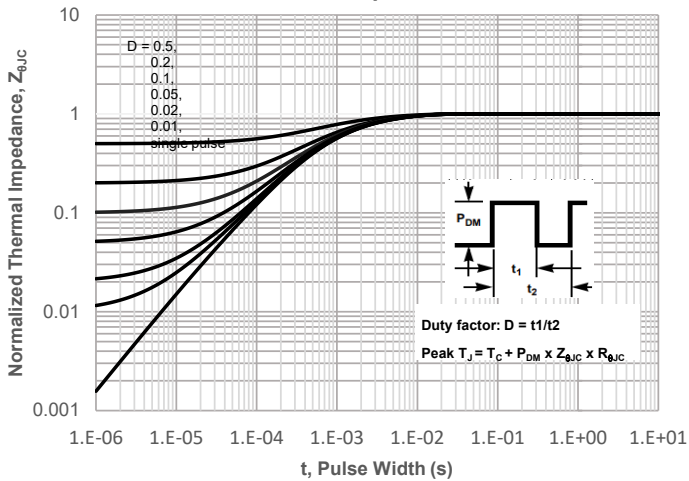
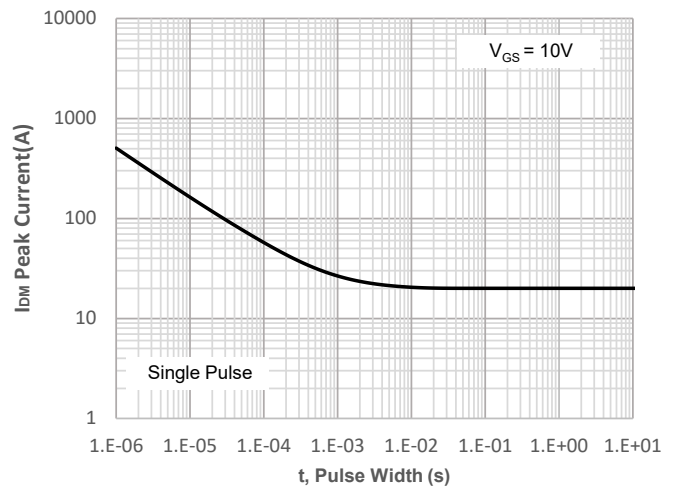


Figure 12: Peak Current Capacity



Test Circuit

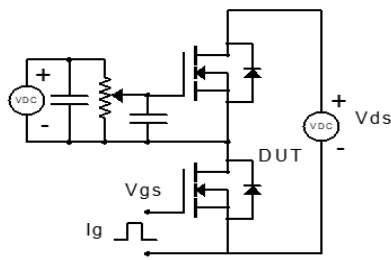


Figure 1: Gate Charge Test Circuit & Waveform

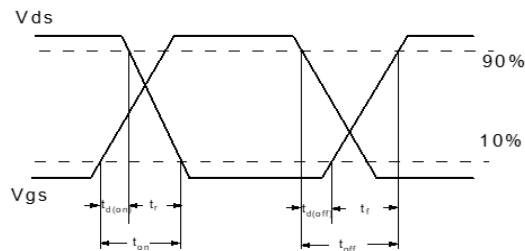
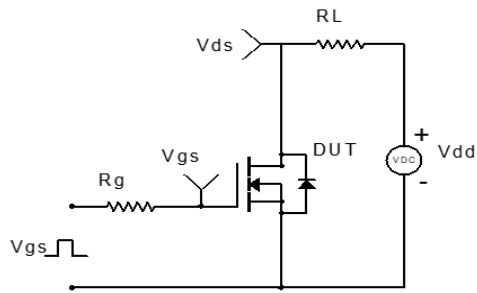


Figure 2: Resistive Switching Test Circuit & Waveform

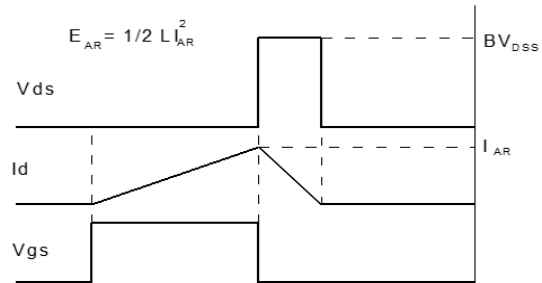
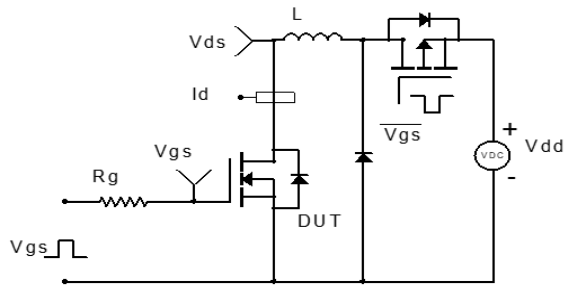


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

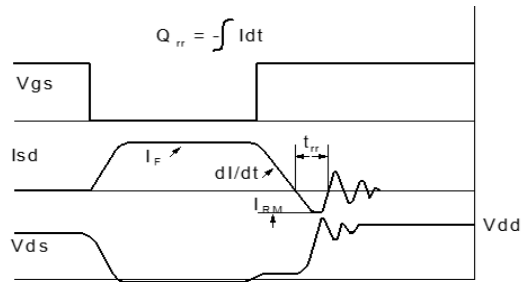
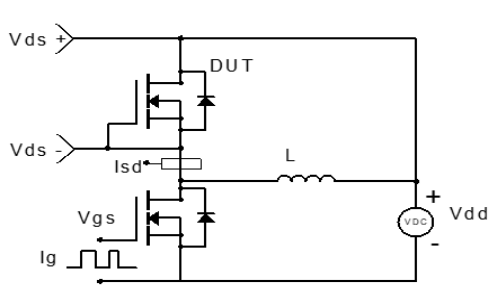
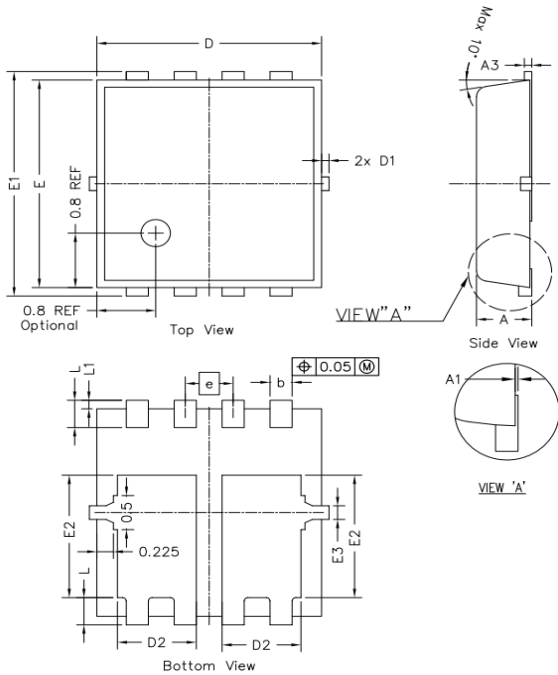


Figure 4: Diode Recovery Test Circuit & Waveform




Package Mechanical Data(PDFN3x3-8L-D)



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	---	---	0.050	----	----	0.002
A3	0.144	0.152	0.202	0.006	0.006	0.008
b	0.250	0.300	0.350	0.010	0.012	0.014
e	0.65 BSC			0.026 BSC		
D	2.950	3.050	3.150	0.116	0.120	0.124
E	2.950	3.050	3.150	0.116	0.120	0.124
D1	---	---	0.125	----	----	0.005
E1	3.200	3.300	3.400	0.126	0.130	0.134
D2	0.970	1.070	1.170	0.038	0.042	0.046
E2	1.700	1.800	1.900	0.067	0.071	0.075
E3	0.150	0.200	0.250	0.006	0.008	0.010
L	0.300	0.400	0.500	0.012	0.016	0.020
L1	0.075	0.125	0.175	0.003	0.005	0.007

Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co.,Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it. Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement. Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.

 is a registered trademark of Jiangsu JieJie Microelectronics Co.,Ltd.
Copyright ©2023 Jiangsu JieJie Microelectronics Co.,Ltd. Printed All rights reserved.